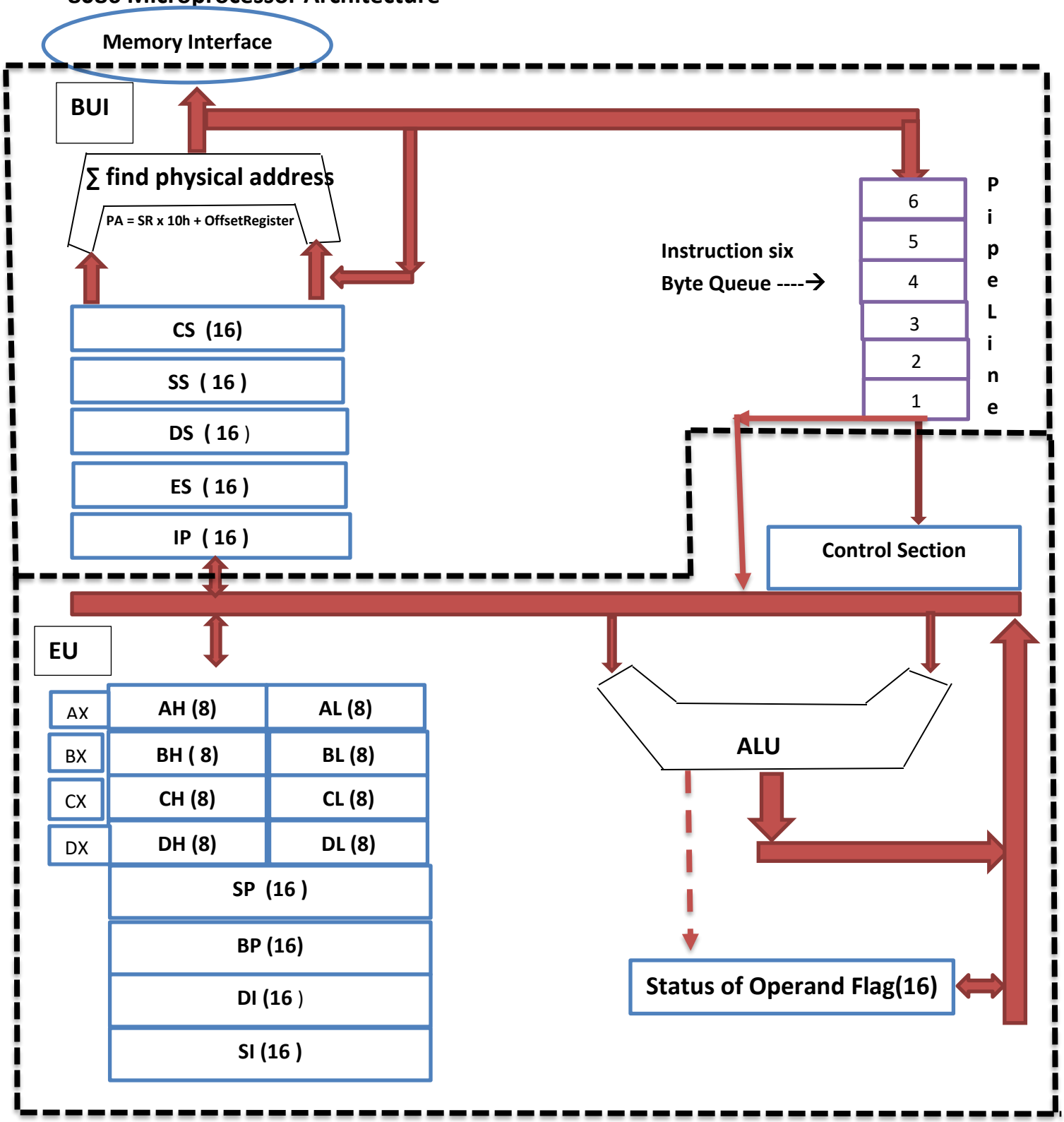
## 8086 Microprocessor Architecture



As a programmer of 8086, we must be familiar with the various register in the BIU bus interface unit and EU execution unit

**Register**

Microprocessor has registers. A processor register (CPU register) is one of a small set of data holding places that are part of the computer processor. A register may hold an instruction, a storage address, or any kind of data (such as a bit sequence or individual characters). Some instructions specify registers as part of the instruction.

**BIU Bus Interface Unit**

BIU is responsible for establishing communications with external peripheral device and memory via system bus.

**Main Purpose of BIU serves is as followed**

1. It fetches the instruction from memory
2. It reads data from IO and Memory
3. It writes data into IO and memory
4. It provides the address relocation facility.

**BIU contains three main parts**

1. Instruction Queue.
2. Segments registers
3. Instruction pointer

**Instruction Queue**

1. BIU pre-fetches six instruction bytes advance from memory
2. The pre-fetched instruction are stored in a group of high speed registers know instruction queue
3. This instruction queue works on FIFO order.
4. BIU and EU works in parallel
5. The simultaneous operations of BIU and EU is possible only when the EU does not require the System bus
6. The process of fetching the next instruction in advance while the EU is executing the current instruction is pipelining

**Segment registers Of BIU**

1. The 8086 MP has the capability of addressing 1MB memory, Which is divided 16 local segments.

2. Each segment contains 64kb memory
3. But any instant 8086 works with only four segments
4. Each segment associated with segment register
    a. Code Segment Register CS-16 bits
    b. Data Segment Register DS-16 bits
    c. Stack Segment Register SS-16 bits
    d. Extra Segment Register ES-16 bits
5. Segment register of BIU is used to store the starting address of memory segment.
6. BIU generates 20 bits address using segment register and offset pointer registers.

**PA = SR x 10h + OffsetPointer**

Instruction Pointer

1. IP hold the address of next instruction which is to be executed next
2. It contains the OFFSET value of next address.

**Execution Unit (EU)**

EU inform BIU from where the next instruction or data to be fetched. The EU performs following functions

1) It picks up the instruction from the instruction queue of BIU.
2) It decode the instructions and then executes the instruction.
3) It updates the status of flag register.

**Control Unit**

1) It is controlling and coordinating all the activities of sub units
2) It fetches, decodes and executes instruction.
3) It gives control signal like read and write etc.

**ALU of EU**

1) It performs all arithmetic and logical operations.
2) Results may be stored in general purpose register or index register.
3) It updates flag register after instructions.

**General Purpose, Pointer and Index Register of EU**

1) EU have four general purpose registers such as AX,BX,CX,DX 16 bits register.
2) These register are used for accessing data very fast.
3) EU have SP and BP for stack segment
4) Index register are SI and DI for data and extra segments, respectively.

**Data Group of register**

General-purpose register also called data group of register.

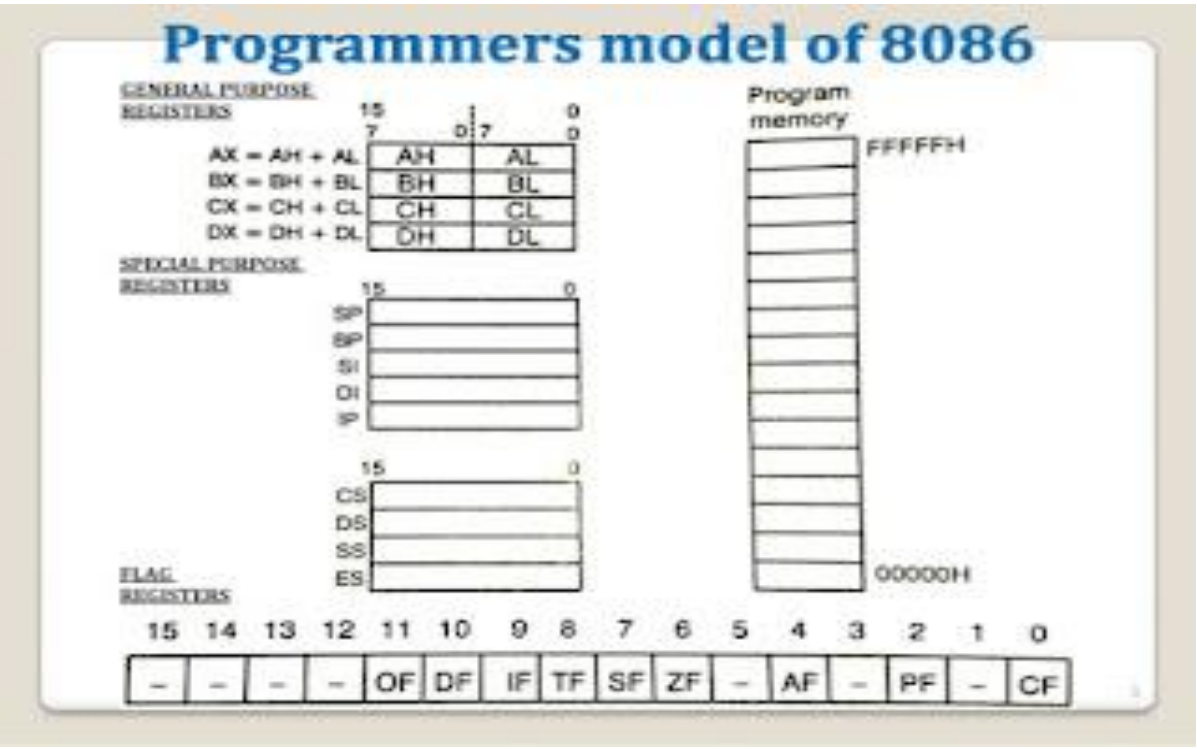
**AX Register (Accumulator):** This is accumulator register. It gets used in arithmetic, logic and data transfer instructions. In manipulation and division, one of the numbers involved must be in AX or AL and AH.

**BX Register (Base Register):** This is base register. BX register is an address register. It usually contain a data pointer used for based, based indexed or register indirect addressing. BX register into divide BL and BH.

**CX Register (Counter register):** This is Count Register. This serves as a loop counter. Program loop constructions are facilitated by it. Count register can also be used as a counter in string manipulation and shift/rotate instruction. CX divide into CL and CH

**DX Register (Data Register):** This is data register. Data register can be used as a port number in I/O operations. It is also used in multiplication and division. DX divide into DL and DH.

**8086 Microprocessor Programming Model**



## Exercise

### Theory Questions.

1. Define data group of register in 8086 Microprocessor.
2. Define memory segmentation of 8086 Microprocessor.
3. Write block diagram of 8086 Microprocessor.
4. Shortly describe BIU and EU.
5. What is formula of find Physical Address?

### Practical Questions.

1. Write assembly code to display your name character by character.

### Objective and MCQs:

1. BIU stand for in 8086 Microprocessor.
   a) Basic Interface Unit
   b) Beginner Interface Unit.
   c) Bus Internet Unit.
   d) Bus Interface Unit

2. In the pipeline has _____ bytes of pre-fetch instruction register.
   a) 4
   b) 6
   c) 2
   d) 3

3. ____ hold the address of next instruction, which is to be executed next.
   a) IP
   b) BP
   c) CS.
   d) DX

4. Each segment of computer memory of 1MB has divide into _____ Kb.
   a) 128Kb.
   b) 512KB.
   c) 64GB.
   d) 64KB.

5. BIU generates ____ bits address using segment register and offset pointer registers.
   a) 16
   b) 8
   c) 20
   d) 32

6. In the 8086-microprocessor data group, register also called _____.
   a) Segment Register
   b) General purpose Register.
   c) Instruction pointer register.
   d) Nothing all

7. The instruction queue registers work on _____ order.
   a) FIFO
   b) LIFO
   c) VIVO
   d) OPPO

8. This is _____ it is serves as a loop counter._____
   a) CS
   b) DS.
   c) CX.
   d) ES.

9. The _____ register show status execution of every instruction.
   a) BX.
   b) DX.
   c) CX.
   d) Flag.

10. The process of fetching the next instruction in advance while the EU is executing the current instruction is _____
    a) Cashed.
    b) Pipelining.
    c) Extra memory.
    d) Nothing all.