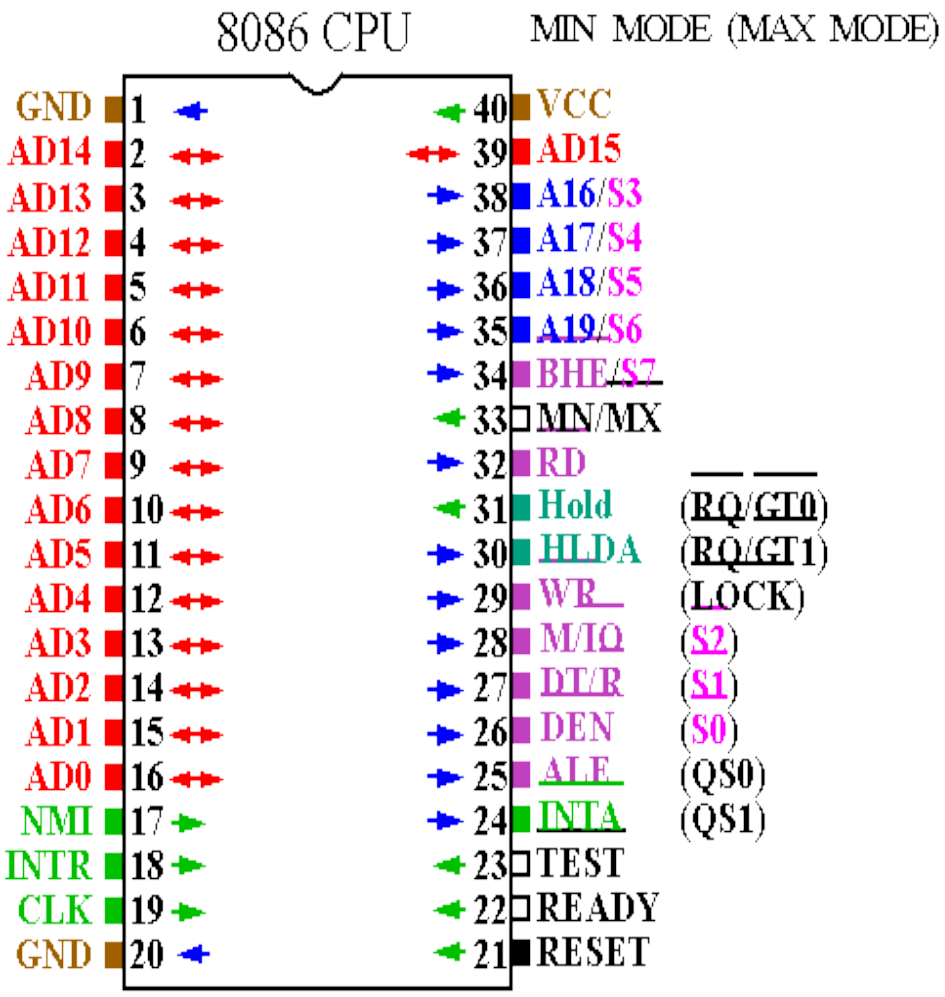
Microprocessor 8086 Pins information

The 8086 was the first 16-bit microprocessor available in 40-pin DIP (Dual Inline Package) chip. Let us now discuss in detail the pin configuration of an 8086 Microprocessor.

Here is the pin diagram of 8086 microprocessor



Let us now discuss the signals in detail –

Power supply and frequency signals
It uses 5V DC supply at VCC pin 40, and uses ground at VSS pin 1 and 20 for its operation. This two ground pins are there to have less power dissipation.

Clock signal/System CLK

Clock signal is provided through Pin-19. It provides internal timing to the processor for operations. Its frequency is different for different versions, i.e. 5MHz, 8MHz and 10MHz.

Address/data bus

AD0-AD15. These are 16 address/data bus. AD0-AD7 carries low order byte data and AD8-AD15 carries higher order byte data. During the first clock cycle, it carries 16-bit address and after that it carries 16-bit data. Here AD0-AD-15 are time multiplexed Address Data lines and can be separate by ALE terminal if ALE=1 then it carries address [AD0-AD15] and if ALE= 0 then it carries data [D0-D15].

Address/status bus

A16-A19/S3-S6. These are the 4 address/status buses. During the first clock cycle, it carries 4-bit address and later it carries status signals. If ALE=1 then it carries Address [A16-A19] and if ALE=0 then it carries status signal [S3-S6].

S3 and S4 indicates which segment register is accessed by 8086 during current bus cycle. S5 reflect IF flag register. S6 is always zero and S7 is always one.

S3	S4	Segment name
0	0	ES
1	0	SS
0	1	CS
1	**1**	**DS**

S7/$\overline{\text{BHE}}$

BHE stands for Bus High Enable. It is available at pin 34 and used to indicate the transfer of data using data bus D8-D15 of D0-D15. This signal is low during the first clock cycle, thereafter it is active.

Read($\overline{\text{RD}}$)

It is available at pin 32 and is used to read signal for Read operation. If it is logic 0, microprocessor reads data from memory or IO devices.

Ready

It is available at pin 22. It is an acknowledgement signal from I/O devices that data is transferred. It is an active high signal. When it is high, it indicates that the device is ready to transfer data. When it is low, it indicates wait state. If the ready pin is at login 1, it has no effect on the operation.

If it is logic 0, 8086 enter into the wait like idle. Because it is used to synchronize slow peripheral devices.

RESET

It is available at pin 21 and is used to restart the execution. It causes the processor to immediately terminate its present activity. This signal is active high or logic 1 for the first 4 clock cycles to RESET the microprocessor. After RESEET of 8086, CS and IP initialized to FFFFh and 0000h, so physical address will be FFFF0h and remaining register to zero.

INTR (Interrupt Request)

It is available at pin 18. It is an interrupt request signal, which is sampled during the last clock cycle of each instruction to determine if the processor considered this as an interrupt or not. This is level

triggered hardware interrupt. If IF = 1, INTR =1, then 8086 gets interrupted and if IF=0 , INTR =1 then INTR is disabled.

NMI
It stands for non-maskable interrupt and is available at pin 17. It is an edge triggered input, which causes highest priority an interrupt request to the microprocessor 8086. It cannot be disabled by the software.

$\overline{\text{TEST}}$
This signal is like wait state and is available at pin 23. When this signal is high or logic 0, then the processor has to wait for IDLE state, else the execution continues. It is used for synchronization.

MN/$\overline{\text{MX}}$
It stands for Minimum/Maximum and is available at pin 33. It indicates what mode the processor is to operate in; when it is high, it works in the minimum mode and vice-versa.
Minimum mode with Vcc and will work as single microprocessor. The maximum mode connected with ground and will works multiple co-processor.

$\overline{\text{INTA}}$ (Interrupt Acknowledgment)
It is an interrupt acknowledgement signal and id available at pin 24 along with interrupt request on INTR. When the microprocessor receives this signal, it acknowledges the hardware/peripherals interrupt.

ALE
It stands for address latch enable and is available at pin 25. A positive pulse is generated each time the processor begins any operation. This signal indicates the availability of a valid address on the address/data lines.

$\overline{\text{DEN}}$
It stands for Data Enable and is available at pin 26. It is used to enable Trans receiver 8286. The trans receiver is a device used to separate data from the address/data bus.

DT/R
It stands for Data Transmit/Receive signal and is available at pin 27. It decides the direction of data flow through the Trans receiver. When it is high, data is transmitted out and vice-a-versa.

M/$\overline{\text{IO}}$
This signal is used to distinguish between memory and I/O operations. When it is high, it indicates I/O operation and when it is low indicates the memory operation. It is available at pin 28.

WR
It stands for write signal and is available at pin 29. It is used to write the data into the memory or the output device depending on the status of M/IO signal.

HLDA

It stands for Hold Acknowledgement signal and is available at pin 30. This signal acknowledges the HOLD signal.

HOLD

This signal indicates to the processor that external devices are requesting to access the address/data buses. It is available at pin 31.

QS1 and QS0

These are queue status signals and are available at from pins 24 to 25. These signals provide the status of instruction queue. Their conditions are shown in the following table −

QS0	QS1	Status
0	0	No operation
0	1	First byte of opcode from the queue
1	0	Empty the queue
1	1	Subsequent byte from the queue

$\overline{S0}$, $\overline{S1}$, $\overline{S2}$

These are the status signals that provide the status of operation, which is used by the Bus Controller 8288 to generate memory & I/O control signals. These are available at pin 26, 27, and 28. Following is the table showing their status −

S2	S1	S0	Status
0	0	0	Interrupt acknowledgement
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

LOCK

When this signal is active, it indicates to the other processors not to ask the CPU to leave the system bus. It is activated using the LOCK prefix on any instruction and is available at pin 29.

$\overline{RQ}$/GT1 and $\overline{RQ}$/$\overline{GT0}$

These are the Request/Grant signals used by the other processors requesting the CPU to release the system bus. When the signal is received by CPU, then it sends acknowledgment. RQ/GT0 has a higher priority than RQ/GT1.

Exercise

Theory Questions.

1. What is purpose of READ and Ready pins of 8086 Microprocessor?
2. How you can define Min and MX pins of 8086 Microprocessor.
3. Write pins diagram of 8086 Microprocessor.

Practical Questions.

1. Write assembly code to input an integer number and character from keyboard and display on the screen.

Objective and MCQs:

1. It uses 5V DC supply at VCC pin ____.
   a) 1
   b) 5.
   c) 40
   d) 10

2. Ground at VSS pin _____.
   a) 1
   b) 6
   c) 20
   d) a and c

3. It is available at pin ___ for the processor considered this as an interrupt or not.
   a) 40
   b) 20
   c) 10
   d) 18

4. It is available at pin 31 use for ____
   a) HLDA.
   b) WR.
   c) TEST.
   d) HOLD.

5. ALE stands for _____and is available at pin 25.
   a) Access latch enable
   b) address latch enable
   c) Active latch enable
   d) Nothing all

6. It stands for write signal and is available at pin ___.
   a) 25
   b) 29
   c) 19
   d) 21
7. This signal indicates to the processor that external devices are requesting to access the address/data buses. It is available at pin 31.
   a) HOLD
   b) HALT
   c) READY
   d) Both a and c

8. If S0 =1 , S1 =1 and S2 =1 then status will be _____
   a) Memory Read
   b) Memory Write.
   c) Passive.
   d) Halt.